IN THE CLAIMS

1. (Currently amended) A method for a wafer level chip scale package (CSP), the method comprising:

providing a semiconductor wafer, the semiconductor wafer including semiconductor chips having chip pads and a passivation layer, the wafer further including scribe lines between the chips;

forming a first patterned dielectric layer on the passivation layer that exposes the chip pads;

forming a second patterned dielectric layer on the first patterned dielectric layer that exposes the chip pads;

forming an embossed ~~portion~~ region on the first patterned dielectric layer, the second patterned dielectric layer, and the passivation layer including a concave portion that exposes a portion of the ~~first patterned dielectric~~ passivation layer where a ball pad is to be formed and a convex portion that is formed from the second patterned dielectric layer;

forming a metal wiring layer on the embossed region directly on the exposed portion of the first patterned dielectric layer, ~~and~~ the exposed portion of the second patterned dielectric layer[[s]], and the exposed portion of the passivation layer ~~including the embossed portion~~, the metal wiring layer being electrically connected to the chip pads;

forming a third dielectric layer on the metal wiring layer; and

removing a portion of the third dielectric layer over the embossed ~~portion~~ region to form a connection hole therein, the connection hole exposing a portion of the metal wiring layer to form the ball pad.

2. (Cancelled)

3. (Currently amended) The method of claim 1, wherein the concave portion comprises a ~~circle~~ substantially cylindrical shape and the convex portion has an annular shape.

4. (Currently amended) The method of claim 1, wherein the convex portion comprises a single discontinuous ring shape.

5. (Previously presented) The method of claim 1, wherein an area of the concave portion is inside the convex portion.

6. (Cancelled)

7. (Previously presented) The method of claim 1, further comprising:

forming a solder ball on the ball pad; and

cutting the semiconductor wafer along the scribe lines.

8. (Cancelled)

9. (Previously presented) The method of claim 3, wherein forming a second patterned dielectric layer comprises exposing a portion of the first patterned dielectric layer inside the annular convex portion.

10. (Currently amended) A method for a wafer level chip scale package (CSP) comprising:

providing a semiconductor wafer, the semiconductor wafer including semiconductor chips each having chip pads and a passivation layer;

forming a first dielectric layer on the passivation layer;

patterning the first dielectric layer to expose the chip pads;

forming a second dielectric layer on the patterned first dielectric layer;

patterning the second dielectric layer to expose the chip pads;

forming an embossed ~~portion~~ region on the first patterned dielectric layer, the second patterned dielectric layer, and the passivation layer;

forming a concave portion in the embossed ~~portion~~ region that includes an exposed portion of the ~~first dielectric~~ passivation layer where a ball pad is to be formed;

forming a convex portion in the embossed ~~portion~~ region ~~of the second dielectric layer~~;

forming a metal wiring layer on the embossed region directly on the exposed portion of the first patterned dielectric layer, ~~and~~ the exposed portion of the second patterned dielectric

layer[[s]], and the exposed portion of the passivation layer, the metal wiring layer being electrically connected to the chip pads;

forming a third dielectric layer on the metal wiring layer; and

removing a portion of the third dielectric layer to form a connection hole therein, the connection hole exposing a portion of the metal wiring layer over the embossed ~~portion~~ region to form a ball pad.

11. (Cancelled)

12. (Previously presented) The method of claim 10, further comprising:

forming a solder ball on the ball pad.

13. (Withdrawn) A wafer level chip scale package (CSP), comprising:

a semiconductor chip having chip pads and a passivation layer exposing chip pads;

a first patterned dielectric layer disposed on the passivation layer; and

a second patterned dielectric layer, the first and second patterned dielectric layers exposing the chip pads,

wherein the first and second patterned dielectric layers have an embossed portion comprising a concave portion and a convex portion, the concave portion exposing a portion of the first patterned dielectric layer where a ball pad is to be formed, the convex portion being formed of the second patterned dielectric layer.

14. (Withdrawn) The apparatus of claim 13, wherein the concave portion comprises a circle shape, and the convex portion comprises a ring shape and having a smaller diameter than the concave portion.

15. (Withdrawn) The apparatus of claim 13, wherein the convex portion comprises a discontinuous ring shape.

16. (Withdrawn) The apparatus of claim 13, wherein the area of the concave portion inside the convex portion is approximately equal to the area of the convex portion.

17. (Currently amended) A method of making a wafer level chip scale package (CSP), the method comprising:

providing a semiconductor wafer, the semiconductor wafer including a semiconductor chip having chip pads and a passivation layer, the wafer further including scribe lines between the chips;

forming a first patterned dielectric layer on the passivation layer that exposes the chip pads;

forming a second patterned dielectric layer on the first patterned dielectric layer that exposes the chip pads, wherein the first patterned dielectric layer, ~~and~~ the second patterned dielectric layer[[s]], and the passivation layer have an embossed ~~portion~~ region comprising a[[n]] ~~annular~~ substantially cylindrical concave portion and an annular convex portion, the concave portion exposing a portion of the ~~first patterned dielectric~~ passivation layer where a ball pad is to be formed, the convex portion being formed of the second dielectric layer;

forming a metal wiring layer on the embossed region directly on the exposed portion of the first patterned dielectric layer, ~~and~~ the exposed portion of the second patterned dielectric layer[[s]], and the exposed portion of the passivation layer, the metal wiring layer being electrically connected to the chip pads;

forming a third dielectric layer on the metal wiring layer; and

removing a portion of the third dielectric layer to form a connection hole that exposes a portion of the metal wiring layer.

18. (Previously presented) The method of claim 3 wherein the convex portion is contained within the concave portion.

19. (Currently amended) The method of claim 18 wherein the convex portion is bounded by substantially vertical side walls and wherein said method further includes forming a ball pad on the concave portion, the convex portion, and the walls.

20. (Cancelled)

21. (Previously presented) The method of claim 5 wherein the area of the concave portion inside the convex portion is approximately equal to an area of the convex portion.